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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Larry Eugene Mosley

Title: MULTI-LAYER CHIP CAPACITOR

Docket No.: 884.240US1

Serial No.: 09/537,274

Filed: March 29, 2000

Due Date: July 29, 2002

Examiner: Eric W. Thomas

Group Art Unit: 2831

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ An Amendment and Response Under 37 CFR 1.111 (6 Pages).
- ☒ Clean Version of Pending Claims (6 pgs.).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: Mark V. Muller
Atty: Mark V. Muller
Reg. No. 37,509

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 8 day of July, 2002.

Jane E. Brockschink

Name

Jane E. Brockschink

Signature

Customer Number 21186

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
(GENERAL)

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S/N 09/537,274



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Applicant: Larry Eugene Mosley

Examiner: Eric W. Thomas

Serial No.: 09/537,274

Group Art Unit: 2854

Filed: March 29, 2000

Docket: 884.240US1

Title: MULTI-LAYER CHIP CAPACITOR

PATENT
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#221
8/1/02

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

The Applicant's representative has reviewed the Office Action mailed on April 29, 2002. Please amend the above-identified patent application as follows, and consider the appended remarks.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect the amendment of previously pending claim 1 to correct a typographical error which prompted an objection due to the resulting informality, and not for reasons related to patentability. The specific amendments to individual claims are detailed in the following marked up set of claims.

1. (Twice Amended) A multi layer integrated circuit capacitor comprising:
 - a substrate;
 - a first conductive layer located over and contacting the substrate;
 - a first insulator layer located over and contacting the first conductive layer, the first insulator layer not contacting the substrate;
 - a second conductive layer located over the first insulator layer;
 - a second insulator layer located over the second conductive layer;
 - a third conductive layer located over the second insulator layer;
 - a third insulator layer located over the third conductor layer; and
 - a plurality of conductive vias downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third [conductor] conductive layers.